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# Concept Report: Microprocessor Control of Electrical Power System

Eugene Perry

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# Concept Report: Microprocessor Control of Electrical Power System

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George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama

National Aeronautics
and Space Administration

**Scientific and Technical
Information Office**

1977

# CONCEPT REPORT: MICROPROCESSOR CONTROL OF ELECTRICAL POWER SYSTEM

## INTRODUCTION

Previous space power systems used analog circuits and devices and man interface for systems control and monitoring. This report describes an electrical power system which uses a microprocessor system to accomplish the same task. A microprocessor-controlled system offers many distinct advantages over the typical system. First, it permits real-time modification of system parameters for optimizing a system configuration, especially in the event of an anomaly. Second, by reducing the components count, the assembling and testing of the unit is simplified, and reliability is increased.

The nucleus of the control system is a programmable large-scale integrated circuit called a microprocessor. As a central processing unit, a microprocessor has basically the same architecture as a large scale computer. A microprocessor has three basic functional building blocks: an arithmetic/logic unit, and instruction decoder, and control and synchronization. Making reference to these building blocks (Fig. 1), a microprocessor may be defined as an integrated circuit capable of performing arithmetical and logical operations under program control in an eight-bit parallel fashion.

Presently, the principal energy sources for long-life spacecraft are silicon solar cell arrays and nickel-cadmium batteries. A typical solar array system (SAS) used in electric power generation is presented in Figure 2. This system is composed of a solar array for supplying electrical power, a battery for energy storage during solar occultation, and a charger and regulator for power processing and sharing. Expansion of the system to meet increased power requirement involves multiple systems operating in parallel such that the total power would be met. A system of this type has been proven reliable and efficient, but it is limited in flexibility.

System flexibility is perhaps the chief advantage of a microprocessor based system. The flexibility is based on the ability to replace hardware with software. If, after finalization of a design, the user requires a system modification, the required alteration could probably be implemented by changing the

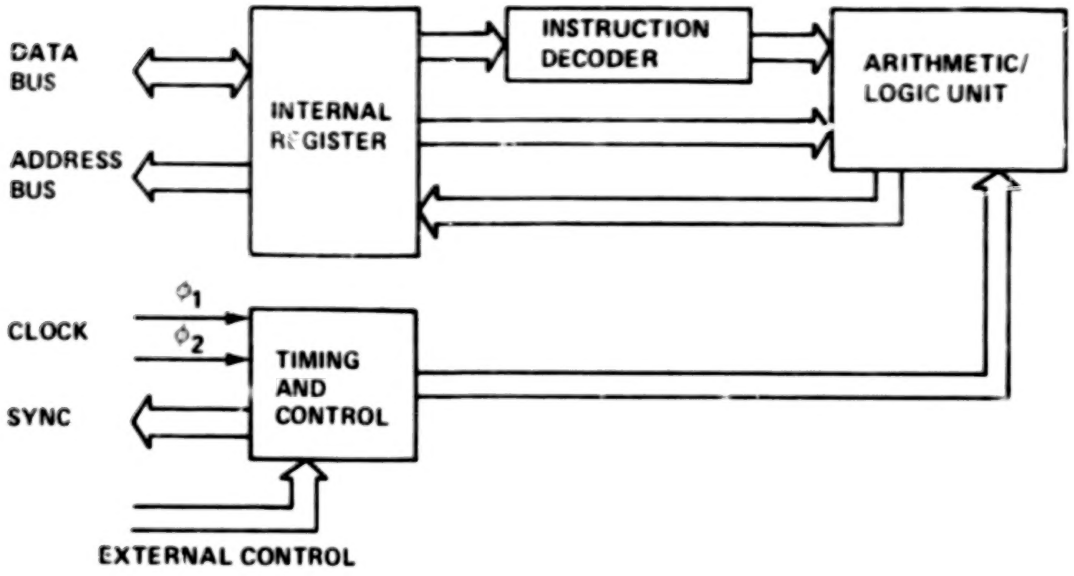



Figure 1. Microprocessor building blocks.

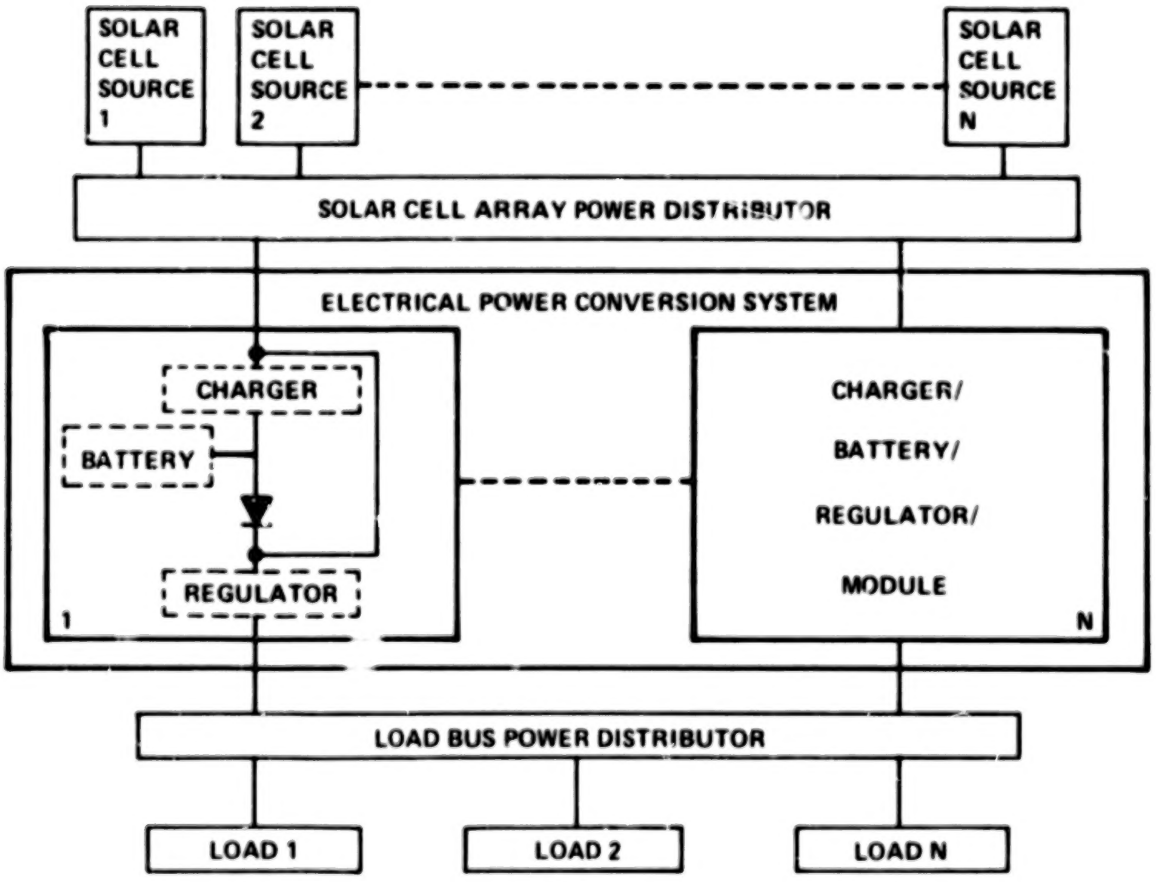



Figure 2. Typical solar array system used in electric power generation.

software only. Such software modification is simple to implement. Once the modified program is written and tested, a new read only memory (ROM) could be programmed to replace the ROM in the design which contained the original program. Such software implementation enhances system capability, facilitates design and system element flexibility, and makes the job of designing faster and less expensive than before.

## SYSTEM DESCRIPTION

Work done in investigating this concept has been directed toward designing and developing a reuseable modular power conversion system capable of satisfying a large percentage of future space applications' requirements. The system was required to have sufficient flexibility for extension to a wide range of applications and various configurations. Other constraints imposed on the power processing system include minimum weight and volume, and no single point failure will result in a system failure. The efforts resulted in a breadboarded model of a programmable power processor system (PPPS).

The PPPS is a multiprocessor electrical power system which uses multiple central processing units in a system configuration, as presented in Figure 3. The system consists of a programmable control (PC) and 2 to 24

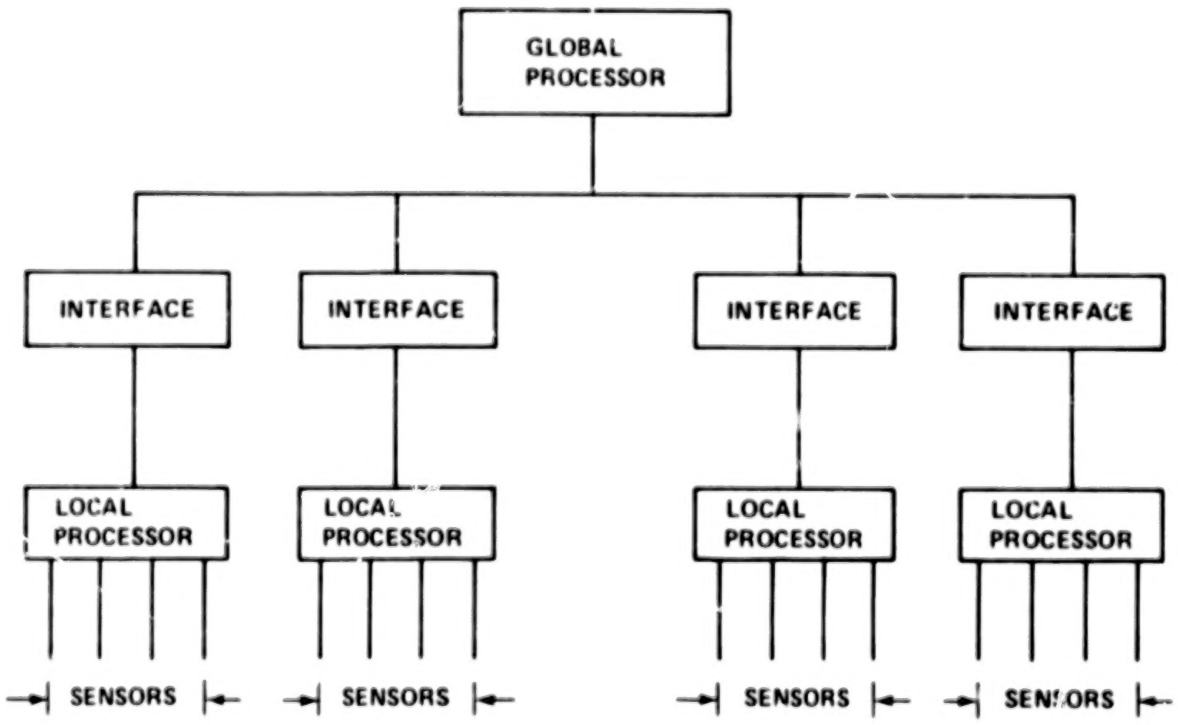



Figure 3. Multiprocessor system.

programmable power processors (PPP). The PC acts as the master controller which supervises the operation of the local processors in a loosely coupled manner. The PPP is a versatile power unit composed of a switching regulator whose operation and function is supervised or controlled by a resident microprocessor-based controller. A PPP is also capable of operating independent of the PC.

As the global controller, the PC handles integration functions such as load sharing, system reconfiguration, and serves as the system communication link for handling telemetry data and commands. The main performance requirement shall be the satisfactory integrated control of multiple PPP for data manipulation, system configuration, and telemetry transfer.

Each PPP is a reuseable power unit whose functional configuration is not limited by hardware design. Under program control, any PPP can be configured as a charger, a constant voltage source or a constant current source, and can perform any voltage/current control functions desired, within the electrical limitation of the power module. A PPP is capable of operating in two distinct modes: (1) the autonomous mode — independent PPP, with its local controller, operating as a programmable power unit and (2) the collective mode — multiple PPP operating as a system under global control.

## PPP DESCRIPTION

The PPP is a versatile dc power system which consists of a power processor (PP), regulator, and a controller/interface (C/I), programmable controller, as shown in Figure 4. The controller, the nucleus of the PPP, provides the building block capability for a flexible system.

The C/I subsystem, Figure 5, consists of a microprocessor chip which interfaces with data, control, and address busses forming an 8-bit microcomputer. The C/I's bus system is formed by a 16 line address bus, a 5 line control bus, and an 8 line bidirectional data bus. The address bus is used to poll a memory location for data or commands. Transfer of data and commands is done via the data bus. The control bus ensures synchronization during data transfers and addressings. The C/I uses random access memory (RAM) for data storage and transfer, and eraseable programmable read only memory (ePROM) for program and subroutine storage. Line driver/receivers are used to reduce noise susceptibility during transmission.

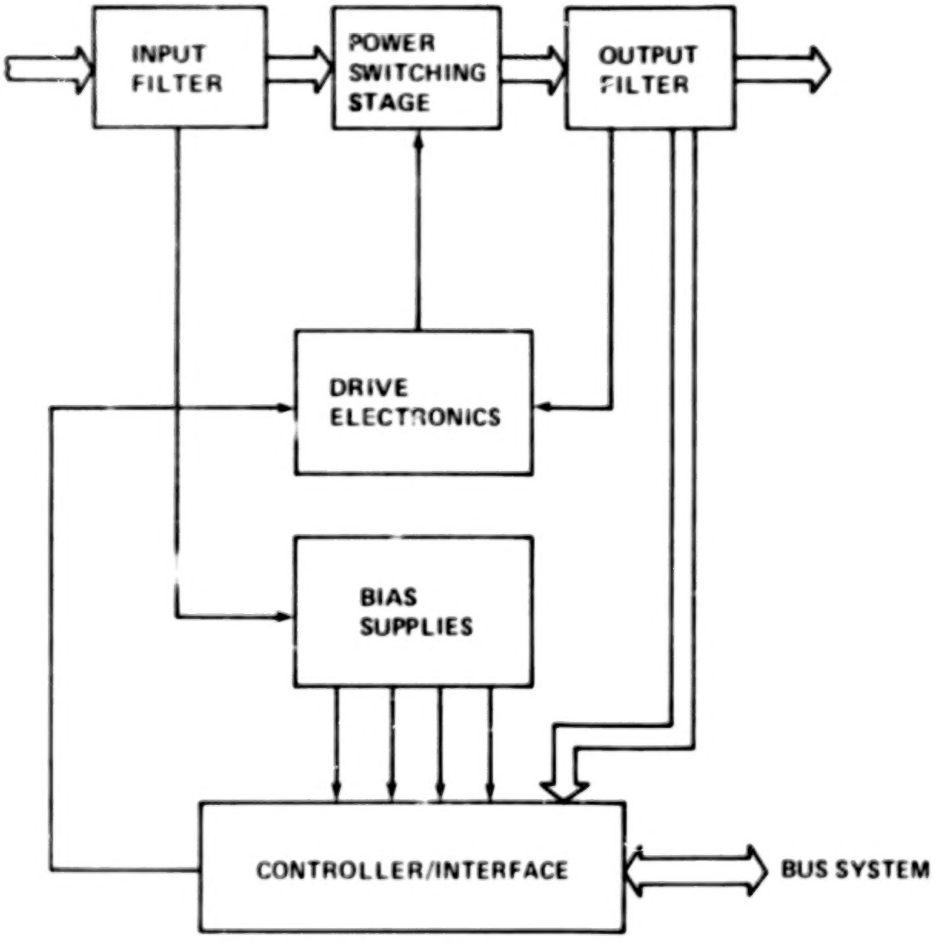



Figure 4. PPP block diagram.

The PP, a step-down switching regulator, is designed to produce output voltages ranging from 4 to 56 Vdc at load currents up to 15 amperes from an unregulated input voltage source ranging from 18 to 130 Vdc. The capability to supply output power to a load over the specified output voltage is shown in Figure 6.

Protective circuitry is included in the PPP to ensure proper operation. Internal circuits limit the output current at 15 amperes under "output short circuit" condition. Conditions that create a hazard to flight or components will cause the regulator to be switched off.

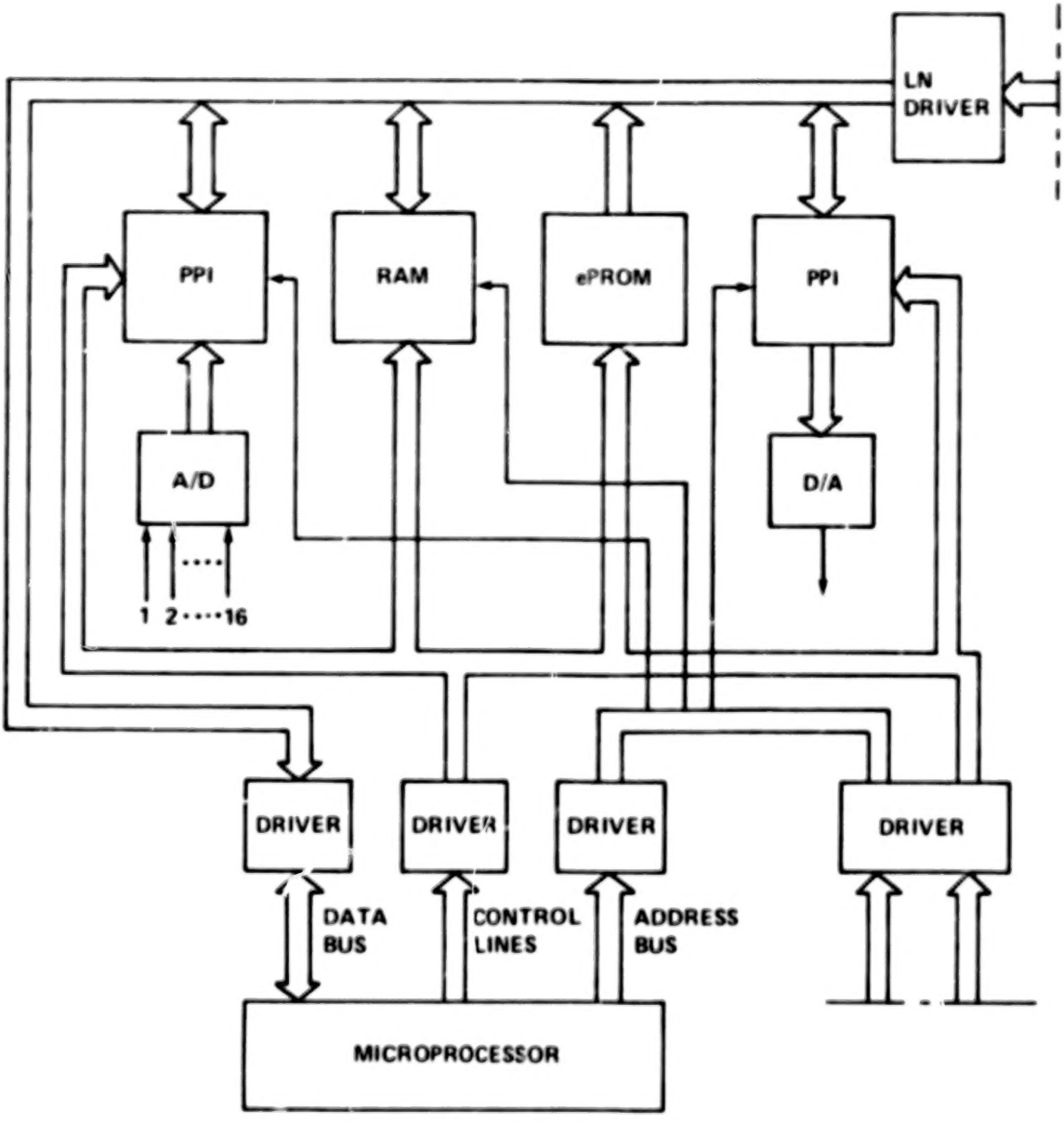



Figure 5. C/I subsystem.

Typical PP operating parameters, Table 1, are monitored with two types of sensors. Voltages are sensed by precision resistor dividers and currents are monitored by current transducers. The range of the sensed output is 0 to 5 Vdc. As currently designed, a maximum of 16 parameters can be monitored by the C/I. Increasing the parameter amount is possible with a minimum effort.

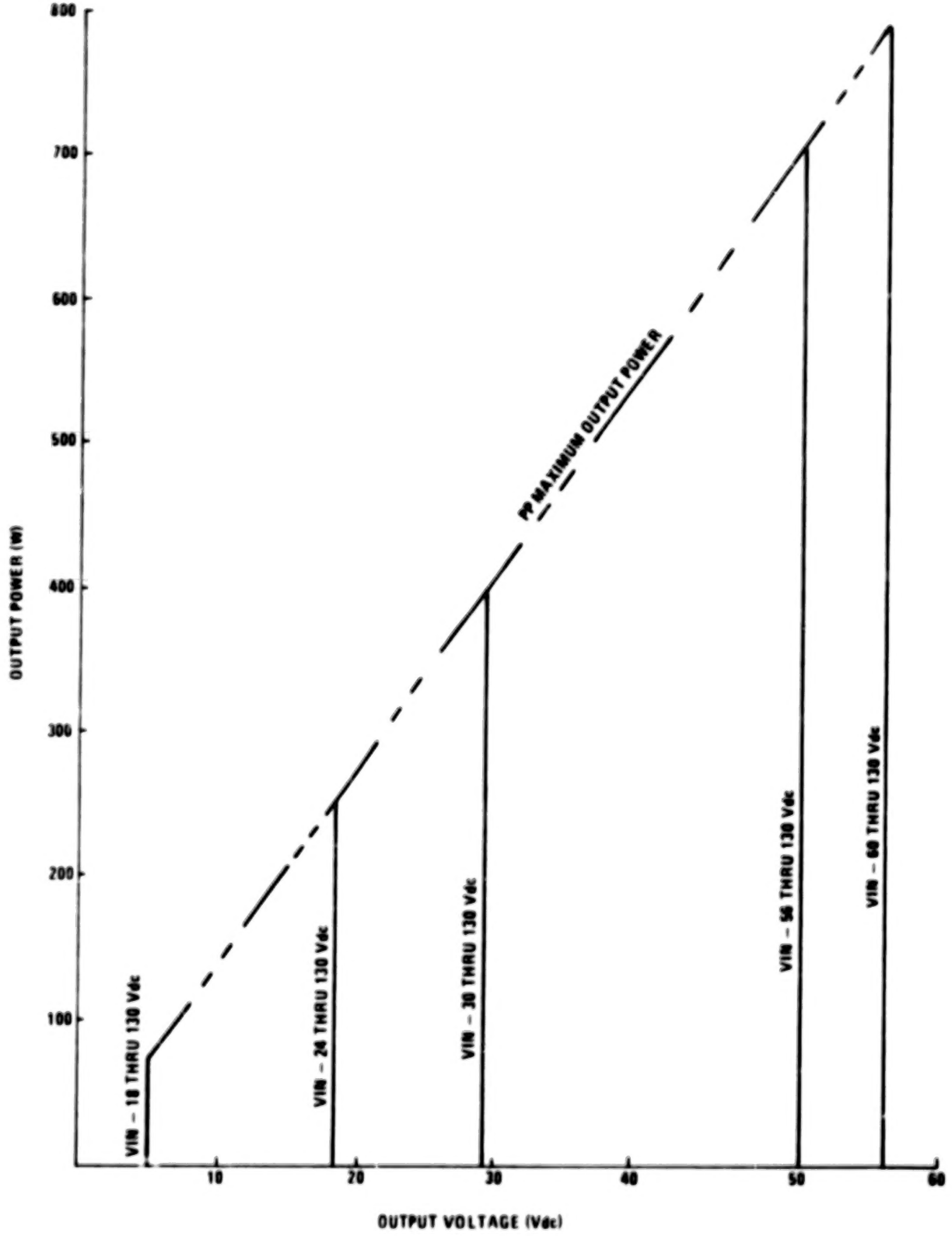



Figure 6. Capability to supply output power to a load over the specified output voltage.

TABLE 1. OPERATING PARAMETERS

| PP Parameter Monitored | Quantity or Range Monitored | Sensor Output (Input to A/D) | Form of Conditioned Data |
|---|---|---|---|
| Input Voltage | 0.0 150.0 Vdc | (TBD) 5.0 Vdc | 12 Bit Digital Word |
| Output Voltage | 0.0 100.0 Vdc | (TBD) 5.0 Vdc | 12 Bit Digital Word |
| Input Current | 0.0 20.0 | (TBD) (TBD) Vdc | |
| Output Current | 0.0 20.0 A | (TBD) (TBD) Vdc | |
| Reference Voltage | 10.0 Vdc | 5.0 Vdc | 12 Bit Digital Word |
| Control Voltage | 0.0 5.0 Vdc | 0.0 5.0 Vdc | |
| Case Temperature (Main Switching Transistor) | (TBD)° C (TBD)° C | (TBD) (TBD) | 12 Bit Digital Word |
| On Off Switching Status | On/Off | (TBD) | 1 Bit Per Switch |

The integration of the PP and the C/I defines a versatile dc power system, with increased flexibility, reliability, and efficiency. System operation becomes a matter of monitoring parameters, evaluating data, and determining the necessary action. Modification of control functions becomes a matter of program instructions manipulation.

A supervisory program (executive) and a collection of various monitoring and control programs are stored in memory. The executive control program calls and executes the monitoring and control programs according to a predetermined sequence, such as data acquisition and command transfers.

Under control of the C/I, analog voltages produced by the PP's sensors are multiplexed into the data acquisition system (DAS) module and converted into a 12-bit digital word, which is transferred and stored in RAM. The C/I then analyzes the stored data to determine the operating condition of the PP, and makes control decisions as to whether a change in the PP's control voltage is necessary.

# PC DESCRIPTION

The PC is a global controller which handles system control and external communication.

The subsystems for the PC are shown in the block diagram of Figure 7. The PC is a microprocessor-controlled unit with the program stored in ePROM and RAM for data storage and transfers. Line driver/receivers are used to ensure transmission accuracy.

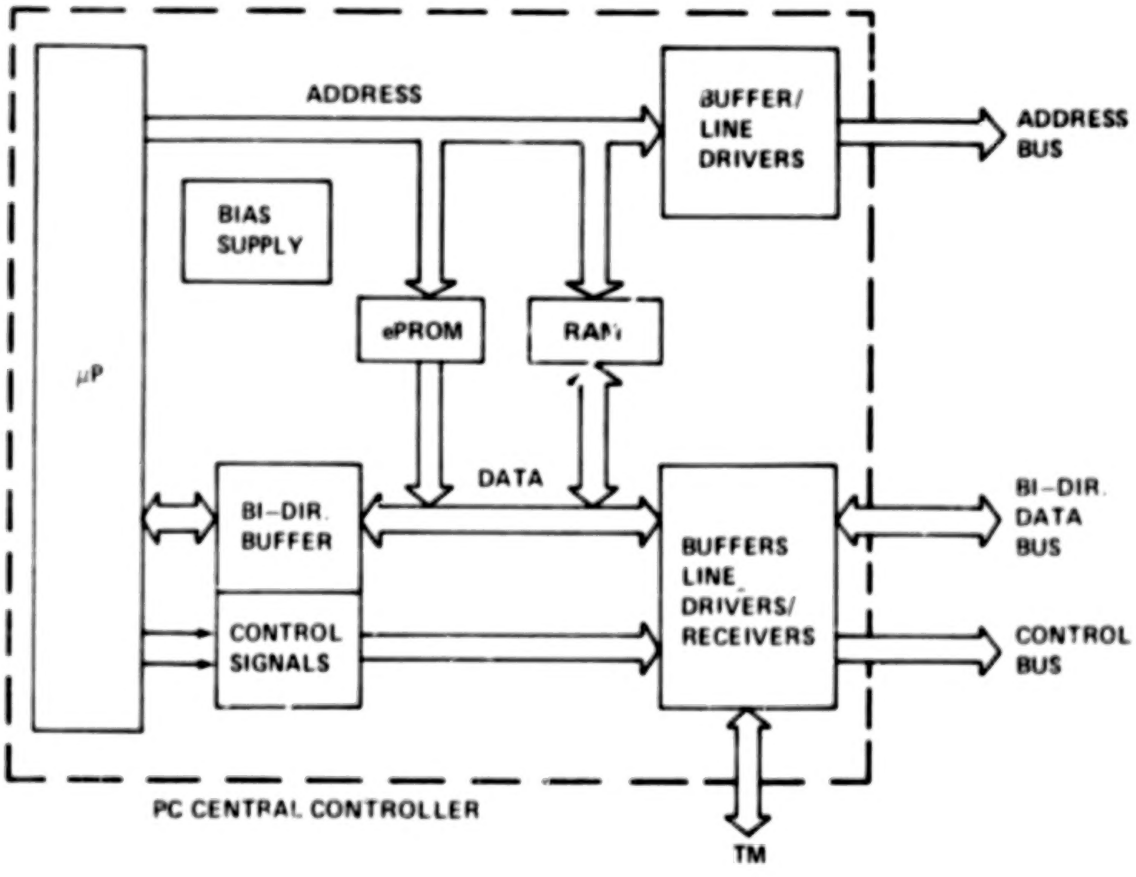



Figure 7. PC block diagram.

The PC bus system consists of an 8-line bidirectional data bus, a 16-line address bus, and a 5-line control bus. All control signals necessary to ensure synchronized operation of the PC and multiple PPP are transmitted via this

microprocessor control bus. All PPP performance data transferred to the PC and all control data transferred from the PC to the PPP are transferred via the 8-line bidirectional data bus. The 16-line address bus is used for addressing any PPP and any memory location of the PC.

Communication between the PC (global controller) and an individual C/I (local controller) is accomplished via the address bus. The transaction between the controller is done by mapping RAM to the interfaces into the memory map for the global controller. This technique is illustrated in Figure 8. Thus, they communicate by transmitting to and retrieving data from common memory.

## SOFTWARE DESCRIPTION

The operational software for the PPPS is composed of an executive control program and various subroutines. After system's initialization, the executive continuously monitors the local system and controls the sequence of events. The general flow chart for the executive is shown in Figure 9.

The program first determines the number of PPP units in the system. After the executive has compiled a list of the PPP's, it then polls each PPP's shared memory for the identifier bytes. The byte is a predetermined code which defines the function of a unit, the program, and the list of the PPP's which are similar and need to be optimized together.

After this initialization by the global processor, the next step is the acquisition of parameters from the PPP by functions. After data acquisition, each group of PPP is optimized. After group optimization, the program will execute any telemetry command. An additional feature is a cycle counter. Using the cycle counter, certain noncritical portions of the control loop of the executive could be executed less frequently than once per cycle. For instance, telemetry need not be transmitted every cycle. Each PPP has a predetermined program similar to the executive.

The operation of a PPP is accomplished by a predetermined software package located in the C/I. This software package placed in ROM defines the function of the PPP. The PPP's initialization occurs prior to the PC's initialization of the C/I. After initialization the C/I performs data acquisition of all necessary parameters. The C/I then computes a control command based on its preassigned function. If the control command is within a predetermined limit, other parameter limits are analyzed to determine if the command should be

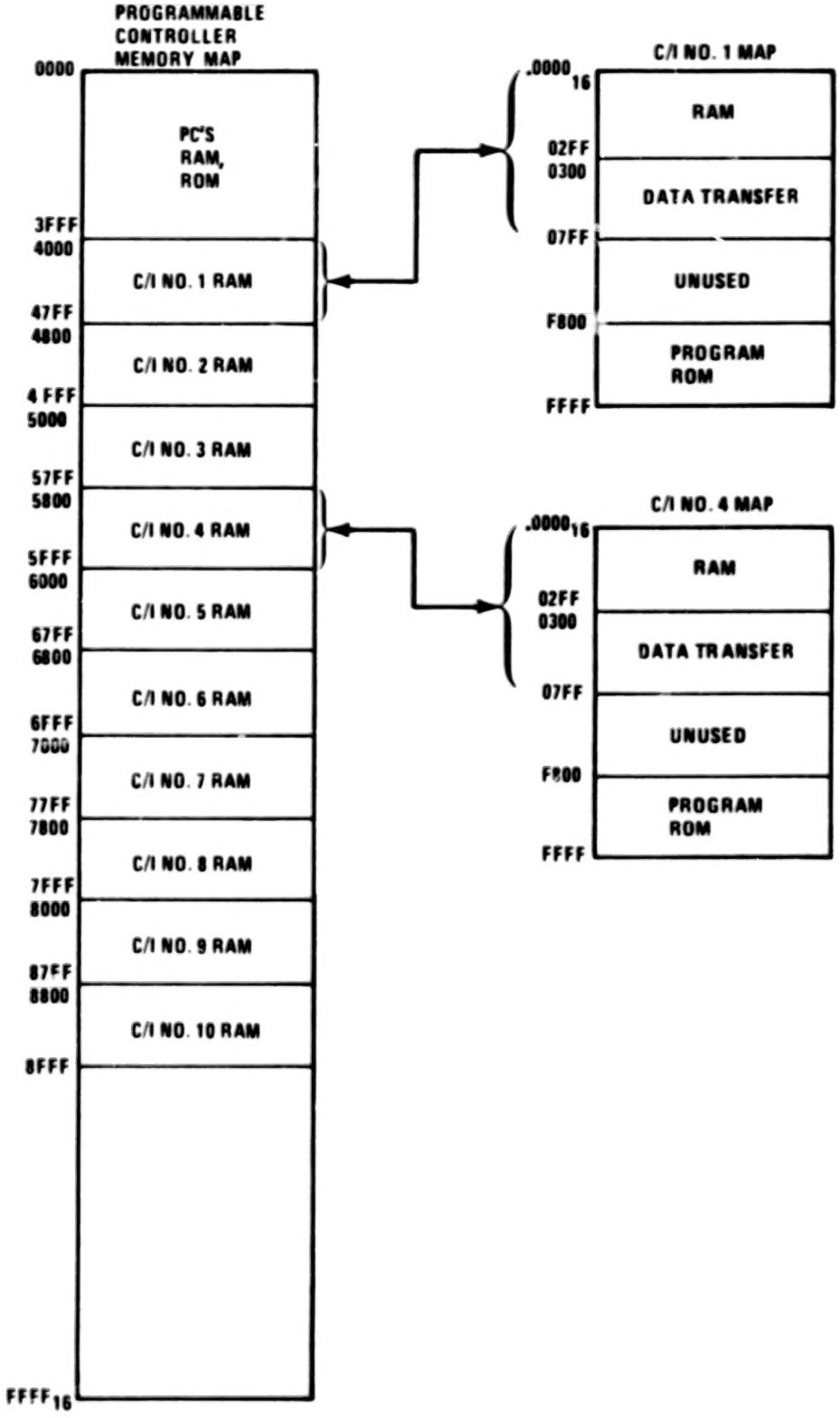



Figure 8. Memory map showing coexistant memory.

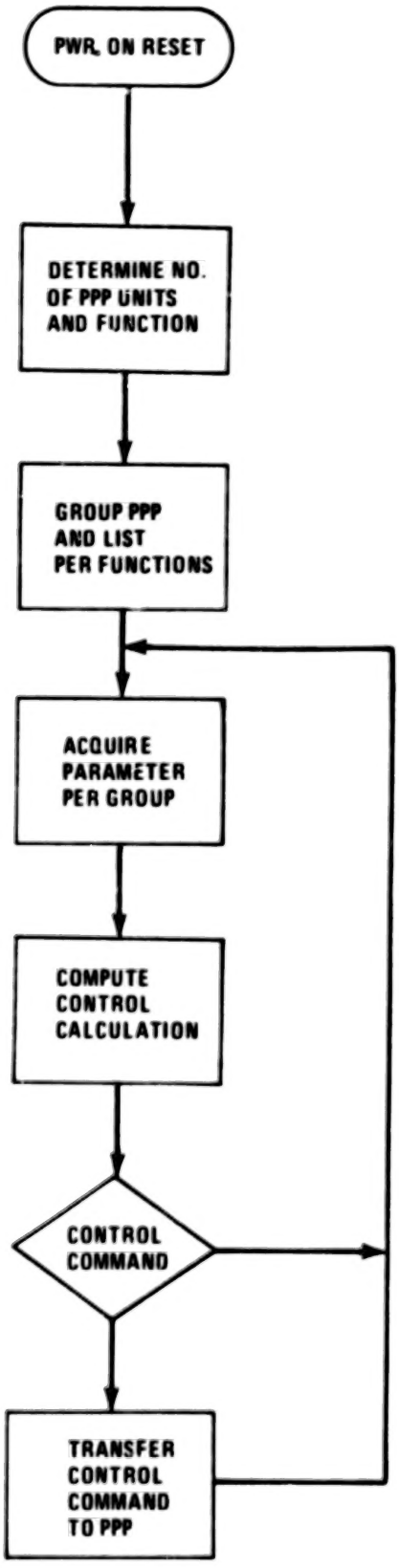

PWR. ON RESET
DETERMINE NO. OF PPP UNITS AND FUNCTION
GROUP PPP AND LIST PER FUNCTIONS
ACQUIRE PARAMETER PER GROUP
COMPUTE CONTROL CALCULATION
CONTROL COMMAND
TRANSFER CONTROL COMMAND TO PPP

Figure 9. General executive flowchart.

modified due to these local conditions: the C/I, the output, the calculated control command to the power unit, and branches back to the data acquisition function. If the C/I was operating in the PPPS configuration, then the C/I would modify the control command as directed by the global modifier prior to power unit transfer.

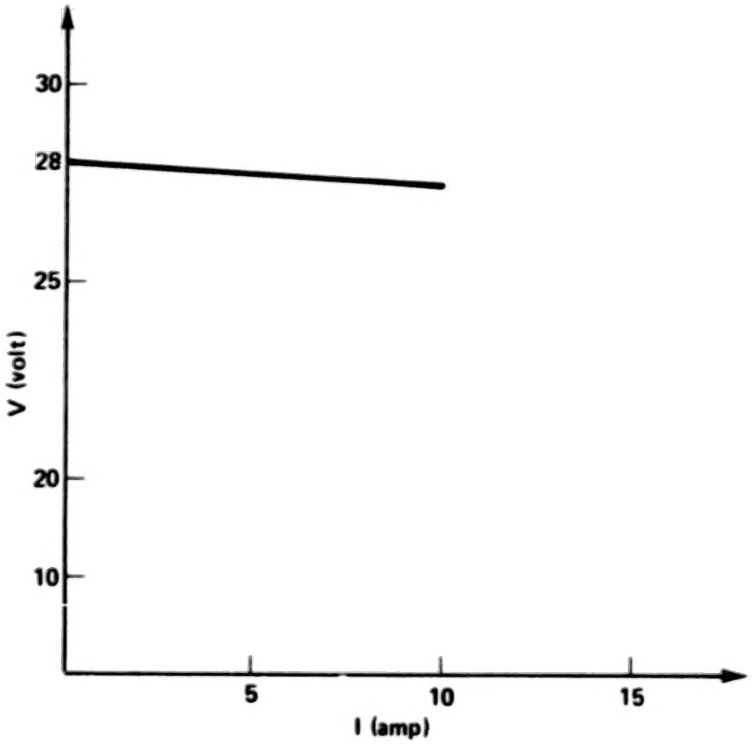
The operational software for the global and local processors is designed for flexibility. The global processor is required to control a maximum of 24 PPP's. Each of the PPP's, however, could be performing different functions or have various parameters (constant current, regulator, charger, etc.). Thus, the software package for any two local processors would probably be different.

These software restrictions are accommodated by flexible program design. A different software package will be developed to perform the various functions. For example, a 28-Vdc regulator program will be developed and placed in ROM. If a power module is to be a 28-Vdc regulator, a regulator ROM is plugged into the C/I. Similar programmed ROM for the other functions will be developed.

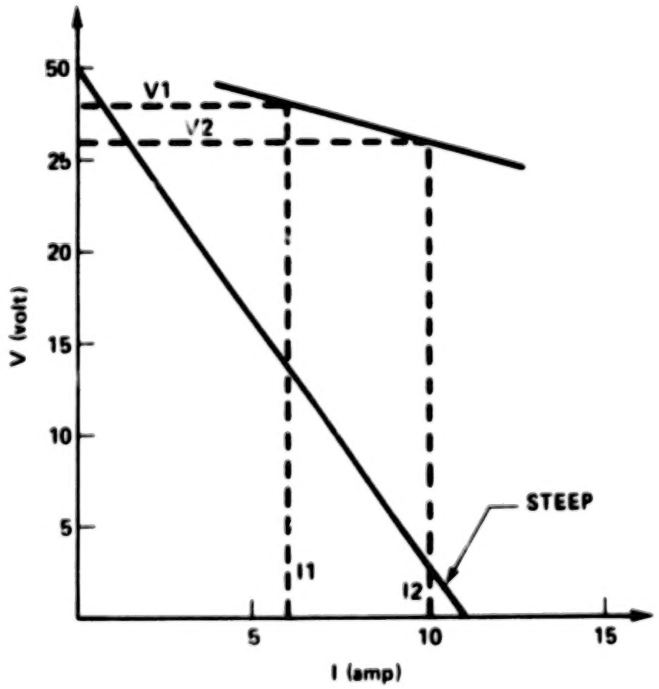
## APPLICATIONS

To illustrate the ease with which control and monitoring functions can be implemented, an examination of the methods developed and tested for accomplishing various power processing tasks is helpful. A PPP operating in the autonomous mode was configured as a constant voltage source. The PPP was programmed to convert the input voltage (30 to 130 Vdc) into a regulated output voltage. Figure 10 depicts the output characteristics of the PPP. The output voltage was maintained between 27.5 Vdc at full load and 28.0 Vdc at no load, with a programmed maximum current of 10 amperes.

Additional software development resulted in a programmable output load slope (POLS) routine, which permits the user to specify the band of operation of the PPP. In the previously mentioned example, the PPP's output voltage varied from 27.5 at full load to 28 Vdc at no load. Using the POLS routine, the output characteristics were modified, as shown in Figure 10b. The PPP's output voltage is now maintained between 26.0 Vdc to 28.0 Vdc. This routine also controls the minimum and the maximum output currents, 7 and 10 amperes, respectively. The operational flowchart for the POLS is shown in Figure 11. In addition to the POLS, there exists a constant current routine which has been tested with a PPP.




a. Constant voltage supply.




b. POLS.

Figure 10. Output characteristics of the PPP.

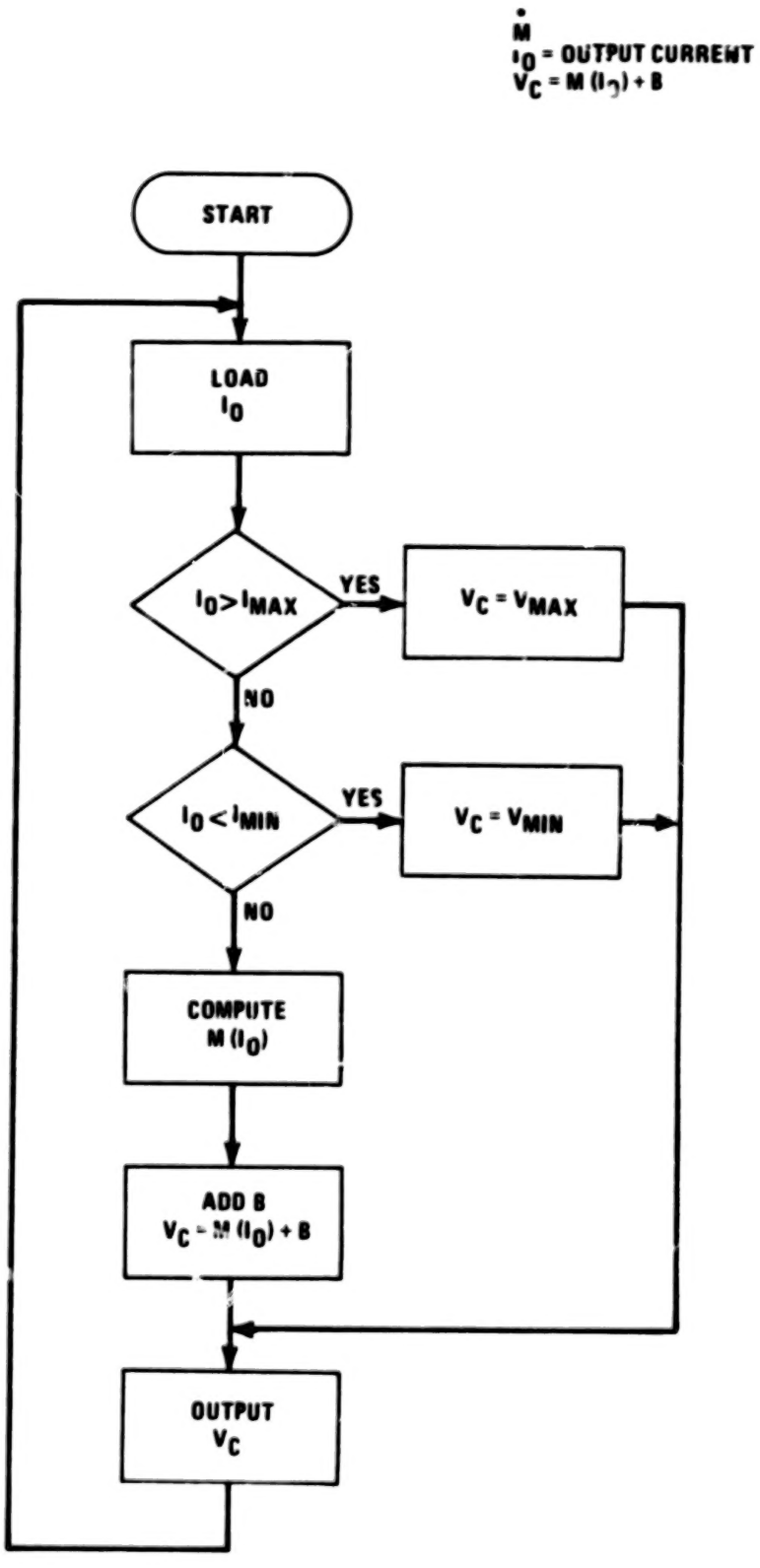



Figure 11. POLS operational flowchart.

The PPPS could replace previous complex power systems, such as the 18 charger battery regulator module (CBRM) which made up the electrical power subsystem of Skylab. Figure 12 shows a block diagram of two distinct electrical power systems supplying power to a bus; one system uses the CBRM while the other employs the PPPS. From a power and efficiency aspect, the PPPS offers no major advantage under normal operating conditions. However, the PPPS is capable of optimizing system configuration and modifying system parameters in the event of an anomaly, such as the loss of a solar array. There is one power processor design rather than two, a charger and regulator. From a control and monitoring aspect, astronaut interface is minimized. The capabilities of this modular, reuseable power system (the PPPS) to supply power defines an optimum power processing system with maximum flexibility, power utilization, and reliability. This concept is expected to result in significant cost savings in electrical power system design over the next decade.

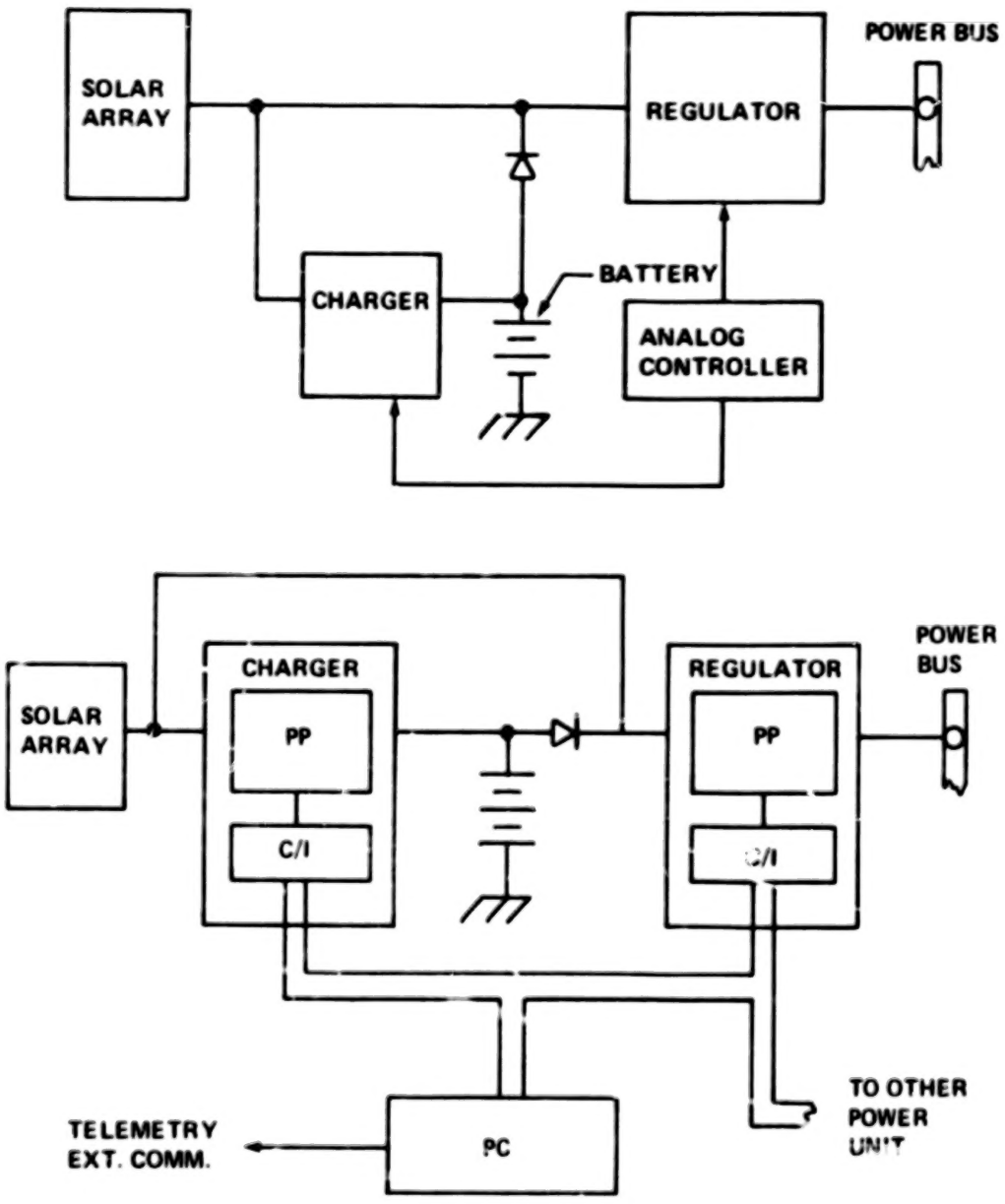



Figure 12. PPPS versus CBRM.

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16. ABSTRACT

To meet the predicted requirements for future programs, it is necessary that new and improved concepts for electrical power generation, conversion, and distribution be developed. The power system should be reuseable and capable of short turn-around times over several missions. Other constraints imposed on the power conversion system include minimum weight and volume, and no single-point failure that will result in a system failure. This report describes the use of microprocessor controllers in space power systems to meet these requirements.

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